What is claimed is:

1. A semiconductor device comprising:

a base;

a semiconductor chip provided on said base and having a first main surface on which a plurality of electrode pads is provided, a surface protecting film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface protecting film and said second main surface;

an insulating extension portion formed so as to surround said side surfaces of said semiconductor chip;

a plurality of wiring patterns electrically connected to said electrode pads and extended from said electrode pads to the surface of said extension portion;

a sealing portion formed on said wiring patterns such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion.

2. The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

3. The semiconductor device according to claim 2,

wherein said electrode posts are formed from a conductive material.

4. The semiconductor device according to claim 3, wherein a thin oxidation layer is formed on a surface of said electrode posts.

5. The semiconductor device according to claim 1, wherein said external terminals are formed as solder balls.

6. The semiconductor device according to claim 1, wherein portions of the wiring patterns on a boundary and vicinity thereof between semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

7. The semiconductor device according to claim 1, wherein said extension portion is formed from an insulating material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

8. The semiconductor device according to claim 7, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a temperature range than glass transition point of less than $1.5 \times 10^{-5}/°C$ and a modulus of elasticity within a range of 7.8 to 22 GPa.

9. A semiconductor device comprising:

a base;

an extension portion having a concave portion which is formed from an insulating material and provided on said base;

a semiconductor chip having a first main surface

on which a plurality of electrode pads are provided, a surface protecting film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface protecting film and said second main surface, which is provided within the concave portion of said extension portion such that said side surfaces are surrounded by said extension portion;

a plurality of wiring patterns electrically connected to each of said electrode pads and extended from said electrode pads to the surface of said extension portion;

a sealing portion formed over said wiring patterns such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided on said wiring patterns in a region including the upper side of said extension portion.

10. The semiconductor device according to claim 9, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

11. The semiconductor device according to claim 10, wherein said electrode posts are formed from a conductive material.

12. The semiconductor device according to claim 10, wherein a thin oxidation layer is formed on a surface of said

electrode posts.

13. The semiconductor device according to claim 9, wherein portions of the wiring patterns on a boundary and vicinity thereof between semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

14. The semiconductor device according to claim 9, wherein said extension portion is formed from an insulating material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

15. The semiconductor device according to claim 14, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a lower temperature range than glass transition point of less than 1.5 $\times 10^{-5}$/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.

16. A semiconductor device comprising:

a base;

an insulating extension portion provided on said base and having a concave portion having inclined inside walls;

a semiconductor chip comprising a first main surface on which a plurality of electrode pads is provided, a surface protecting film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface protecting film and said second main surface, which is provided within the concave portion of said

extension portion such that said side surfaces are surrounded by said extension portion;

an insulating film formed over the surface of said inside walls, the surface of said extension portion, and said surface protecting film such that a part of said electrode pads is exposed;

a plurality of wiring patterns formed on said insulating film, electrically connected to said electrode pads, and extended from said electrode pads to the surface of said extension portion;

a sealing portion formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion.

17. The semiconductor device according to claim 16, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

18. The semiconductor device according to claim 17, wherein said electrode posts are formed from a conductive material and a thin oxidation layer is formed on a surface of said electrode posts.

19. The semiconductor device according to claim 16, wherein said extension portion is formed from an insulating

material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

20. The semiconductor device according to claim 19, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a lower temperature range than glass transition point of less than 1.5 $\times 10^{-5}$/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.